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MCANDREWS HELD & MALLOY, LTD
500 WEST MADISON STREET
SUITE 3400
CHICAGO, IL 60661

EXAMINER	
CAMPOS, YAIMA	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Advisory Action Before the Filing of an Appeal Brief	Application No. 10/750,523	Applicant(s) SO ET AL.	
	Examiner Yaima Campos	Art Unit 2185	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 19 December 2007 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.
   b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).

4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☒ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: 12-44.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See Continuation Sheet.
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08) Paper No(s). _____
13. ☐ Other: _____.

Continuation of 11. does NOT place the application in condition for allowance because: FIRST POINT OF ARGUMENT
Regarding Applicant's remarks that the Examiner has not responded to Applicant's arguments as it appears that the Examiner replicates arguments to various claims without providing a specific response to a claim; the Examiner respectfully disagrees and would like to point out that the Examiner has cited specific portions from the prior art of record that read on the claimed limitations. The Examiner has also grouped claims and arguments that pertain to essentially the same subject matter.
SECOND POINT OF ARGUMENT
In response to Applicant's remark that the feature "reducing the size of a translation lookaside buffer" had not been given patentable weight since it was recited in the preamble of Claim 1; the Examiner would like to point out that after this limitation was incorporated in the body of the pending claims, it has been taken into consideration and examined accordingly.
In response to Applicant's remark that Hinton does not disclose reducing the size of the TLB; the Examiner disagrees and submits that Hinton discloses this limitation as ["Mini-TLB (TWB)," defined as "A small 3-entry instruction mini TLB (6)" (Columns 5-6, lines 62-67 and 1-5) which is of mini/reduced size. Applicant should note that by using "a single bit having a first value or a second value, the single bit providing for translation of even-number pages for which the single bit has a first value and for odd-number pages for which the single bit has the second value" (Columns 1-2, lines 64-67) wherein even-number pages will only be written within "physical register 0 - 106" and odd-number pages will only be written within "physical register 1 - 104;" therefore, having a single entry for each page depending on the value of bit 12 and implementing a TLB of reduced size or mini-TLB, as claimed (See Figures 3 and 7 and related text)].
THIRD POINT OF ARGUMENT
Regarding Applicant's remark that the TWB disclosed by Hinton performs only write operations and not reading and writing as required by the claims; the Examiner disagrees as Hinton discloses ["the logical registers in the TWB compare bits 13 to 31 of this logical address with their stored values 204. If they compare, it is a TWB hit (206). The control logic selects one of these register's hit signals, depending on the value of logical address bit 12 (208)" (Col. 7, lines 25-25) (which comprises reading from the TWB; which corresponds to Applicant's claimed TLB) wherein if the instruction is a TWB miss, "then the TWB stores away the logical and physical address in one of its entries (232). This is the mechanism by which the TWB is loaded" (Figure 7 and related text) (which comprises writing into the TWB; which corresponds to Applicant's claimed TLB)]. Hinton also explains "first and second logical registers in said TWB resulting in a first hit signal with respect to said first logical register or a second hit signal with respect to said second logical register... F. gating to a physical address bus a stored value in one of said first or second physical address registers associated with said selected hit signal (which comprises reading from on of the registers of TWB, as claimed)... issuing a machine bus fetch, upon a condition that said upper order bits of said logical address do not equal a stored value in said first or second logical register in said TWB;... M storing in said TWB said logical address and said second physical address upon a condition that said lower order bits are identical (which comprises writing into one of the registers TWB, as claimed)" (Col. 7, line 54-Col. 8; line 45).
FOURTH POINT OF ARGUMENT
Regarding Applicant's argument that Hinton does not disclose storing even and odd page frame numbers into a single page frame number field of said translation lookaside buffer as Hinton discloses two separate registers; this argument has been considered and is not persuasive.
First of all, the Examiner would like to point out that Applicant's Specification describes storing even and odd page frame numbers into a single page frame number field of said translation lookaside buffer as ["Figure 3 is a relational block diagram illustrating an organizational structure of a mini- TLB system 300 in accordance with an embodiment of the invention. The mini-TLB system 300 comprises a miniature version of the previously mentioned translation lookaside buffer described in Figure 1 (herein termed a mini-TLB 304) communicating with a number of mini-TLB registers 308 and a control processor 324. In one embodiment, the mini-TLB 304 is configured by way of instructions executed by the control processor 324. For the mini-TLB 304 shown in Figure 3, the index and page mask registers function in the same manner as was described earlier in Figure 1. In addition, virtual addressing is performed using the addressing format described in Figure 2, in which a 32 bit virtual address is used. Of course, it is contemplated that in other embodiments, virtual addressing may be performed using more or less than 32 bits. In the embodiment shown, the entry Hi 312 register of Figure 3 facilitates storage and read out of a virtual page number associated with bits [31:12] of the virtual addressing format discussed previously. Hence, as illustrated in Figure 3, the virtual page number (VPN) may be either read from or written into a VPN field (or section) 316 of the mini-TLB 304. The VPN is associated with a page frame number (PFN) which is similarly either read from or written into a PFN field 320 of the mini-TLB 304 using the registers shown (i.e., entry Lo0 or entry Lo1 registers). In the embodiment illustrated in Figure 3, only one of the entry Lo registers (either entry Lo0 or entry Lo1) is valid for use during a write operation; for example, the contents of a valid entry Lo register is written into the page frame number (PFN) field 320 associated with a specified page table entry of the mini-TLB 304. In one embodiment, the least significant bit (lsb) of a VPN (i.e., bit 12 of the 32 bit virtual address described) is used to determine whether the entry Lo0 or an entry Lo1 register contains valid data for writing into the PFN field 320 of the mini-TLB 304. Similar principles may be applied during a read from the mini-TLB 304. For example, the least significant bit (lsb) of the VPN may be used to determine which register, either entry Lo0 or entry Lo1, will be used to access valid page frame number data utilized by the control processor 324 during a read operation. In a read operation, for example, the least significant bit (lsb) of a virtual page number is used to store data into either the entry Lo0 register or the entry Lo1 register. In this fashion, both even and odd page frame numbers may be stored or recalled from a single page frame number field of the mini-TLB 304" (Applicant's Specification, Paragraph 0026)]. Therefore, Applicant's Specification discloses two registers and reading/writing to only one of these two registers when reading/writing to TLB. Emphasis added on underlined portions.
Hinton discloses this limitation as ["Mini-TLB (TWB)," defined as "A small 3-entry instruction mini TLB (6)" (Columns 5-6, lines 62-67 and 1-5) to provide access to memory wherein "the instruction pointer is comprised of logical address bits including upper order bits, lower order bits, and a single bit having a first value or a second value, the single bit providing for translation of even-number pages for which the single bit has a first value and for odd-number pages for which the single bit has the second value" (Columns 1-2, lines 64-67 and 1-29; Column 6, lines 37-63; Figure 3) "TWB" (mini TLB) (Figure 3, Diagram of TWB) in which "a logical address (81) is separated into three parts... Bit 12 selects which of the two entries in the TWB are to be used for this address... Registers (106) marked "0" are for even-numbered 4KB pages, addresses for which bit 12 is a zero. Registers (104) marked "1" are for odd-numbered 4KB pages,

addresses for which bit 12 is a one" (Column 6, lines 37-63) wherein for a TWB load, "one set (even or odd) of the TWB registers in loaded with the logical and physical addresses" (Column 7, lines 5-14). Hinton also explains "first and second logical registers in said TWB resulting in a first hit signal with respect to said first logical register or a second hit signal with respect to said second logical register... F. gating to a physical address bus a stored value in one of said first or second physical address registers associated with said selected hit signal (which comprises reading from on of the registers of TWB, as claimed)... issuing a machine bus fetch, upon a condition that said upper order bits of said logical address do not equal a stored value in said first or second logical register in said TWB;... M storing in said TWB said logical address and said second physical address upon a condition that said lower order bits are identical (which comprises writing into one of the registers TWB, as claimed)" (Col. 7, line 54-Col. 8; line 45).

Therefore, even logical and physical address set is read from/written to TWB and odd logical and physical address set are read from/written to TWB. Therefore, Hinton discloses writing and reading even and odd page frame numbers into a single page frame number field".

For example, when bit 12 is a 0, TWB (Translation Write Buffer or mini-TLB) will read and write in a single field within Physical Register 0 (which is used for even pages), which comprises reading and writing even page frame numbers into a single page frame number field of a translation lookaside buffer. For further explanation, when bit 12 is a 1, TWB will read and write into a single field within Physical Register 1 (which is used for odd pages), which comprises reading and writing odd page frame numbers into a single page frame number field. Therefore, Hinton discloses, "writing and reading even and odd page frame numbers into a single page frame number field" of a translation lookaside buffer, as claimed by Applicant].

FIFTH POINT OF ARGUMENT

Regarding the following remark:

The Examiner states that Hinton discloses "reading from on(e) [sic] of the registers of (Hinton's) TWB, as claimed." However, the Examiner is incorrect, since the claimed invention does not recite registers within a buffer. For example, Hinton does not teach the "first storage register" and "second storage register," as recited in Claim 18 because Hinton's registers are contained within a buffer (i.e., the TWB). Furthermore, the Examiner is requested to review the supporting specification, at Figure 3, which clearly illustrates the relationship of the claimed translation lookaside buffer (TLB) and the registers. As illustrated in Figure 3, the TLB does not comprise the registers. Hence, the Examiner does not show a teaching of what is recited in at least Claim 18, for example. Likewise, the Examiner does not show a teaching of the pending claims. Therefore, the pending claims should be passed to allowance.

The Examiner would like to point out that claims must be given the broadest reasonable interpretation during examination and limitations appearing in the specification but not recited in the claim are not read into the claim (See M.P.E.P. 2111 [R-1]) and claim 18, for example, does not recite any limitations regarding the location of a first register and a second register.

SIXTH POINT OF ARGUMENT

Regarding Applicant's remark that Hinton does not disclose "using a virtual page number;" the Examiner does not agree as Hinton discloses ["logical address (81)" (Col. 6, lines 37-63)].

CONCLUSION

It appears to the Examiner that Applicant's arguments for various claims refer to the same alleged deficiencies in the prior art of record as in previous responses; therefore, these arguments have been addressed in prior office actions (either in rejection to claims or as response to Applicant's arguments). However, those arguments are not persuasive as the Examiner believes the prior art of record reads on the claimed limitations. (Refer to Final Office Action mailed on 10/29/2007) .

SANJIV SHAH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100